IN THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Canceled)

2. (Canceled)

3. (Currently Amended) A method of forming an interlayer dielectric film in a semiconductor device, the method comprising:

forming a conductive layer pattern on a semiconductor substrate including a junction region and an isolation region;~~and~~

forming ~~an~~ insulating film ~~spacer~~ spacers on ~~a sidewall~~ sidewalls of said conductive layer pattern ~~through a common process~~ to expose the junction region;

burying a conductive material between said insulating film spacers;

removing said conductive material and said insulating film ~~spacer~~ spacers in ~~a~~ the isolation region ~~other than a contact plug formation region~~; and

forming an interlayer dielectric film on an entire surface of the semiconductor device so that the interlayer dielectric film is buried between the conductive layer pattern in the isolation region.

4. (Currently Amended) The method of according to claim 3, wherein said conductive layer pattern ~~comprises one of~~ includes a word line ~~and a bit line~~.

5. (Canceled)

6. (Canceled)

7. (Currently Amended) A method of forming an interlayer dielectric film in a semiconductor device, the method comprising:

forming conductive layer patterns and ~~an~~ insulating film ~~spacer~~ spacers on ~~a~~ ~~sidewall~~ sidewalls of said conductive layer patterns on a semiconductor substrate to expose a first contact plug;

burying a conductive material between said ~~conductive layer patterns~~ insulating film spacers;

removing said conductive material and the insulating film spacers at a removal region such that said conductive material remains ~~at remaining regions~~ on the first contact plug to form a second contact plug and the insulating film spacers remain at both sides of the second contact plug; and

burying an interlayer dielectric film between said conductive layer patterns at said removal region.

8. (Currently Amended) The method according to claim 7, wherein ~~at least one of~~ said conductive layer pattern ~~comprises one of a word line and~~ includes a bit line.

9. (New) A method of forming an interlayer dielectric film in a semiconductor device, the method comprising:

forming first conductive layer patterns on a semiconductor substrate including a junction region and an isolation region;

forming first spacers on the first conductive layer patterns;

forming a first interlayer dielectric film on the entire surface;

forming a first contact hole by patterning the first interlayer dielectric film to expose the junction region;

forming a first contact plug by burying a first conductive material in the first contact hole;

forming second conductive layer patterns on the entire surface including the first contact plug;

forming second spacers on the second conductive layer patterns;

forming a second conductive material on the entire surface to bury the second conductive material between the second conductive layer patterns;

forming a second contact plug by leaving the second conductive material on the first contact plug and removing the second conductive material and the second spacers on the first interlayer dielectric film, wherein the second spacers remains at both sides of the second contact plug; and

forming a second interlayer dielectric film on the entire surface;

10. (New) The method according to claim 9, wherein the first conductive layer patterns comprise a word line.

11. (New) The method according to claim 9, wherein the second conductive layer patterns comprise a bit line.

12. (New) The method according to claim 9, wherein the second conductive material includes polysilicon.

13. (New) The method according to claim 9, wherein the second conductive layer patterns further include nitride film.

14. (New) The method according to claim 9, the method further comprising:

performing a first planarization process to remove the second conductive material on the second conductive patterns after forming the second conductive material.

15. (New) The method according to claim 9, the method further comprising:

performing a second planarization process after forming the second interlayer dielectric film on the entire surface.

16. (New) The method according to claim 9, wherein the first spacers remain at both sides of the first contact plug.